Exhibit 21

JEDEC STANDARD

PMIC50x0 Power Management IC Specification, Rev 1.0

JESD301-1

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

2.2 Common Features summary

Table 1 — PMIC Device Type Summary

Device Type	SWA	SWB	SWC	SWD	Unit
PMIC5000 - Current Capability per Phase	5	5	5	5	A
PMIC5010 - Current Capability per Phase	3	3	3	3	A

- VIN_Bulk input supply range: 4.25 V to 15.0 V
- VIN_Mgmt input supply range: 3.0 V to 3.6 V
- Four step down switching regulators: SWA, SWB, SWC & SWD
- Programmable dual phase and single phase regulator for SWA and SWB
- 3 LDO regulators: VBias, VOUT_1.8V, VOUT_1.0V
- Automatic switchover from VIN_Mgmt input supply to VIN_Bulk input supply
- Error injection capability
- Persistent Error log registers
- Secure mode and programmable of operation
- Independently programmable output voltages, power up and power down sequence for switch regulators
- Input and output power good status reporting mechanism
- VIN_Bulk input supply protection feature: Input over voltage
- Output switch regulators protection feature: Output over voltage, output under voltage, output current limiter
- Output current and power measurement, output current threshold mechanism
- Temperature measurement, temperature warning threshold, critical temperature shutdown
- Multi Time Programmable Non-Volatile Memory
- Programmable and DIMM specific registers for customization
- General Status Interrupt Function
- Flexible Open Drain IO (I^2C) and Push Pull (I3C Basic) IO Support

7 Example Schematic

Figure 9 shows an example schematic when PMIC is configured in dual phase regulator mode. Table 26, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, C27, C29, C30, C31 represents the lump sum of distributed capacitance across the entire DIMM.

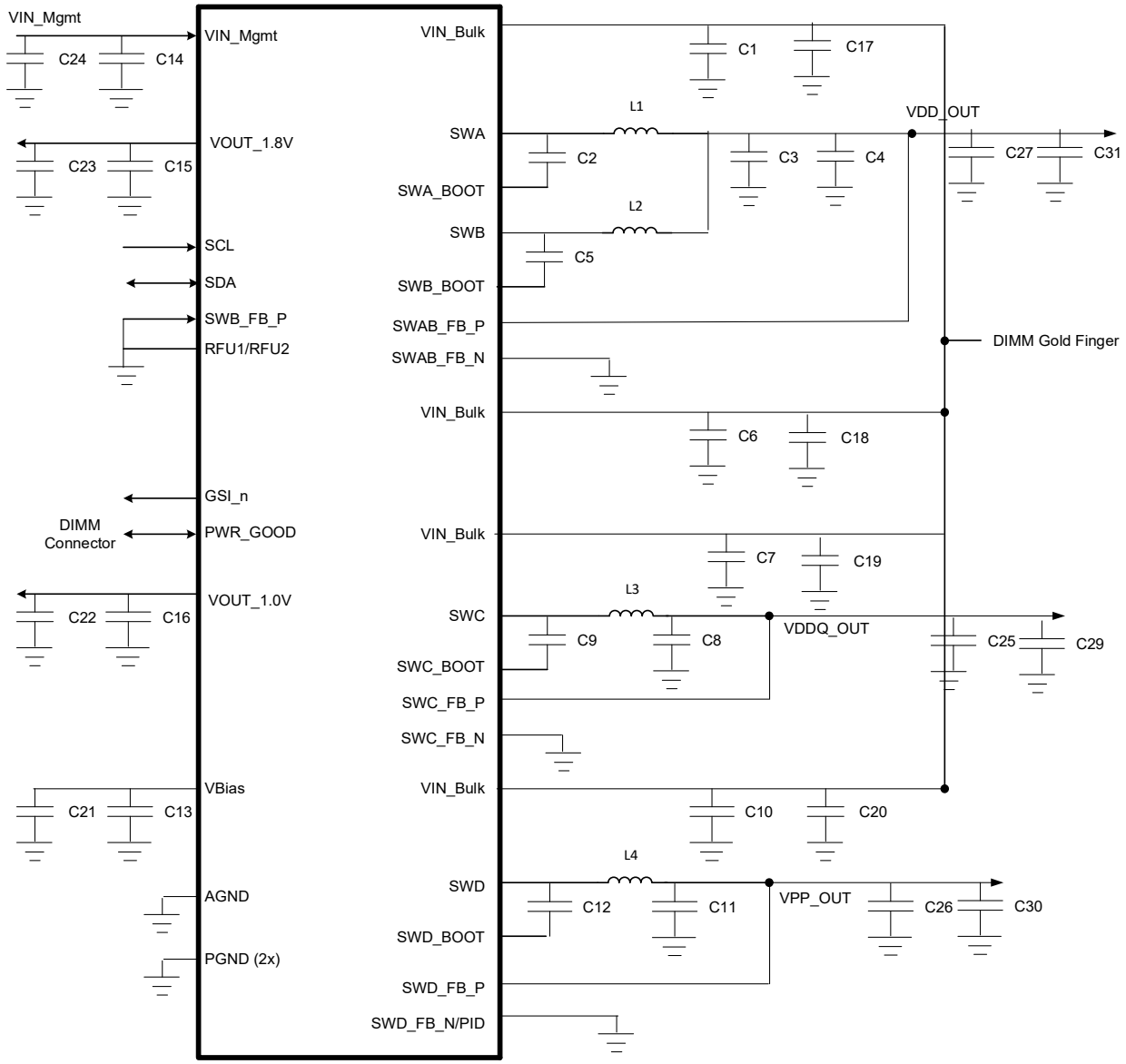

Figure 9 — Dual Phase Regulator Example Schematic

Figure 10 shows an example schematic when PMIC is configured in single phase regulator mode. Table 26, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, C27, C28, C29, C30, C31 and C32 represents the lump sum of distributed capacitance across the entire DIMM.

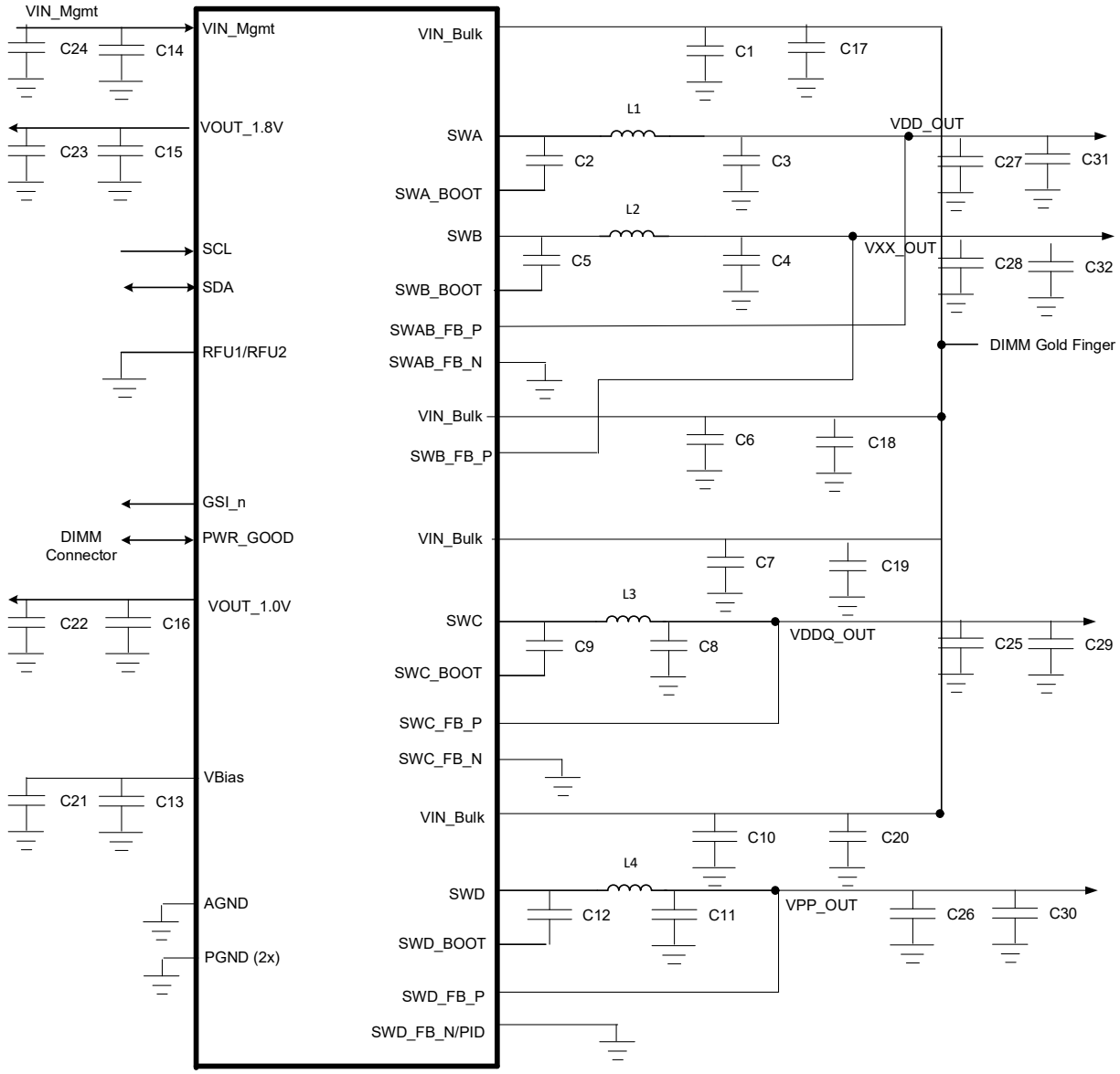

Figure 10 — Single Phase Regulator Example Schematic

Table 30 — Events Interrupt Summary

Event	Status Bit	Clear Bit	Mask Bit	Threshold Bits	Trigger VR Disable?	PWR_GOOD Output	GSI_n Output
VIN_Bulk Power Good	R08 [7]	R10 [7]	R15 [7]	R1A [7:5]	No	Low	Low
VIN_Bulk Over Voltage	R08 [0]	R10 [0]	R15 [0]	R1B [7]	Yes	Low	Low
VIN_Mgmt Over Voltage	R08 [1]	R10 [1]	R15 [1]	R1B [5]	No	High	Low
SWA Output Power Good	R08 [5]	R10 [5]	R15 [5]	R21 [1:0]; R22 [7:6]	No	Low	Low
SWB Output Power Good	R08 [4]	R10 [4]	R15 [4]	R23 [1:0]' R24 [7:6]	No	Low	Low
SWC Output Power Good	R08 [3]	R10 [3]	R15 [3]	R25 [1:0]; R26 [7:6]	No	Low	Low
SWD Output Power Good	R08 [2]	R10 [2]	R15 [2]	R27 [1:0]; R28 [7:6]	No	Low	Low
1.8 V LDO Power Good	R09 [5]	R11 [5]	R16 [5]	R1A [2]	No	Low	Low
1.0 V LDO Power Good	R33 [2]	R14 [2]	R19 [2]	R1A [0]	No	Low	Low
VBias LDO Power Good	R09 [6]	R11 [6]	R16 [6]	R1A [3]	No	Low	Low
SWA Output Over Voltage	R0A [7]	R12 [7]	R17 [7]	R22 [5:4]	Yes	Low	Low
SWB Output Over Voltage	R0A [6]	R12 [6]	R17 [6]	R24 [5:4]	Yes	Low	Low
SWC Output Over Voltage	R0A [5]	R12 [5]	R17 [5]	R26 [5:4]	Yes	Low	Low
SWD Output Over Voltage	R0A [4]	R12 [4]	R17 [4]	R28 [5:4]	Yes	Low	Low
SWA Output Under Voltage	R0B [3]	R13 [3]	R18 [3]	R22 [3:2]	Yes	Low	Low
SWB Output Under Voltage	R0B [2]	R13 [2]	R18 [2]	R24 [3:2]	Yes	Low	Low
SWC Output Under Voltage	R0B [1]	R13 [1]	R18 [1]	R26 [3:2]	Yes	Low	Low
SWD Output Under Voltage	R0B [0]	R13 [0]	R18 [0]	R28 [3:2]	Yes	Low	Low
VBias LDO Output or VIN_Bulk Input Under Voltage	R33 [3]	R14 [3]	R19 [3]	Vendor Specific	Yes	Low	Low
SWA Output Current Limit	R0B [7]	R13 [7]	R18 [7]	R20 [7:6]	No	High	Low
SWB Output Current Limit	R0B [6]	R13 [6]	R18 [6]	R20 [5:4]	No	High	Low
SWC Output Current Limit	R0B [5]	R13 [5]	R18 [5]	R20 [3:2]	No	High	Low
SWD Output Current Limit	R0B [4]	R13 [4]	R18 [4]	R20 [1:0]	No	High	Low
SWA Output High Current/Power	R09 [3]	R11 [3]	R16 [3]	R1C [7:2]	No	High	Low
SWB Output High Current/Power	R09 [2]	R11 [2]	R16 [2]	R1D [7:2]	No	High	Low
SWC Output High Current/Power	R09 [1]	R11 [1]	R16 [1]	R1E [7:2]	No	High	Low
SWD Output High Current/Power	R09 [0]	R11 [0]	R16 [0]	R1F [7:2]	No	High	Low
High Temperature Warning	R09 [7]	R11 [7]	R16 [7]	R1B [2:0]	No	High	Low
Critical Temperature	R08[6]	N/A	N/A	R2E [2:0]	Yes	Low	Low
VIN_Mgmt to VIN_Bulk Switchover	R09 [4]	R11 [4]	R16 [4]	R2F [7]	No	High	Low
Valid VIN_Mgmt in Switchover State	R33 [4]	R14 [4]	R19 [4]	N/A	No	High	Low
PEC Error	R0A [3]	R12 [3]	R17 [3]	N/A	No	High	Low
Parity Error	R0A [2]	R12 [2]	R17 [2]	N/A	No	High	Low

The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or PWR_GOOD signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or PWR_GOOD signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. Table 31 and Table 32 shows the PMIC's response of GSI_n signal and PWR_GOOD output signal for each event before and after host issues the Clear command. The Table 31 and Table 32 assumes that all mask bits are either '0' or '1' for simplicity.

8.14 Input Power Good Status

There is one possibility where PMIC recognizes the input supply fail.

1. VIN_Bulk goes below the threshold set in register Table 121, “Register 0x1A” [7:5].

When this event occurs for a period longer than tInput_PWR_GOOD_GSI_Assertion time then PMIC sets the register Table 103, “Register 0x08” [7] and drives GSI_n and PWR_GOOD output signal as shown in Table 30 at the same time. The PMIC allows access to all registers and PMIC continues to operate as normal as long as VIN_Bulk input remains above 4.25 V. See also Section 8.18. The host is responsible for taking any specific action. The host may clear the VIN_Bulk input power good status register by writing ‘1’ to register Table 103, “Register 0x08” [7] or by writing ‘1’ to global status clear register Table 115, “Register 0x14” [0]. If the input power not good condition is still present then PMIC will continue to drive GSI_n and PWR_GOOD output signal as in Table 30 and the status register Table 103, “Register 0x08” [7] will remain at ‘1’. If the input power not good condition persists, the host may set the appropriate mask register to remove GSI_n or PWR_GOOD output signal as shown in Table 31 and Table 32.

Note that after VR enable command, when VIN_Mgmt input goes below the threshold set in register Table 142, “Register 0x2F” [7], it is reported as switchover event as described in Section 8.22. Prior to VR Enable command, the VIN_Mgmt is always required to be above 2.8 V to guarantee PMIC’s functionality as described in Section 8.2.

8.15 Input Over Voltage Protection

An input over voltage protection mechanism is implemented to limit the voltages to the PMIC. The PMIC actively monitors the input voltage VIN_Bulk and VIN_Mgmt rail.

There are two possibilities where PMIC recognizes the input over voltage event.

1. VIN_Mgmt input goes above the threshold set in register Table 122, “Register 0x1B” [5].
2. VIN_Bulk input goes above the threshold set in register Table 122, “Register 0x1B” [7].

When either one or both event occurs for a period longer than tInput_OV_GSI_Assertion time then PMIC sets the register Table 103, “Register 0x08” [1:0] accordingly and drives GSI_n output signal as shown in Table 30 at the same time. Note that at this point, the PMIC does not assert PWR_GOOD output signal. The PMIC allows access to all registers and PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may clear the VIN_Mgmt or VIN_Bulk input over voltage status register by writing ‘1’ to register Table 111, “Register 0x10” [1:0] appropriately or by writing ‘1’ to global status clear register Table 115, “Register 0x14” [0]. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register Table 103, “Register 0x08” [1:0] will remain at ‘1’.

In programmable mode (i.e., Table 142, “Register 0x2F” [2] = ‘1’), if VIN_Bulk input supply over voltage condition persists greater than tInput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts PWR_GOOD signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the VIN_Bulk input over voltage status register as well as any other relevant status registers individually or by writing ‘1’ to global status clear register Table 115, “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register Table 103, “Register 0x08” [0] will remain at ‘1’. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC’s output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal and input over voltage condition is no longer present.

14.2 Register Map Breakdown

Table 96 — Register Map Breakdown

Register Range	Region	Comments
0x00 - 0x3F	Host Region	Host Accessible Registers
0x40 - 0x6F	DIMM Vendor Region	DIMM Vendor Registers - Non Volatile Memory Allows DIMM vendors to program the PMIC for a given DRAM/DIMM vendor designs. These are password protected registers and password is selected by DIMM vendor. Under normal operation, these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'. These registers require complete power cycle before it takes in effect. Changing these registers under normal operation is considered an illegal operation.
0x70 - 0xFF	Vendor Specific Region	Vendor Specific Registers - Non Volatile Memory These are vendor specific password protected registers. Under normal operation these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'.

14.3 Register Memory Protection

The PMIC DIMM vendors registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to DIMM vendor registers are blocked unless it is unlocked by providing the correct password. The default password for DIMM vendor registers is 0x9473. The PMIC offers DIMM vendors to select their own password for DIMM vendor registers.

14.3.1 Steps to Access DIMM Vendor Region Registers

The steps to access the DIMM vendor registers are as following:

1. Write to register Table 149, "Register 0x37" = 8 bit password LSB code.
2. Write to register Table 150, "Register 0x38" = 8 bit password MSB code.
3. Write to register Table 151, "Register 0x39" = 0x40.
4. Perform Read operations to DIMM vendor registers as desired.
5. Write to register Table 151, "Register 0x39" = 0x00.

14.3.2 Steps to Change DIMM Vendor Region Password

By default, the DIMM vendor region register password is 0x9473. The steps to change the password from default password are as following:

1. Write to register Table 149, "Register 0x37" = 0x73.
2. Write to register Table 150, "Register 0x38" = 0x94.
3. Write to register Table 151, "Register 0x39" = 0x40.
4. Write to register Table 149, "Register 0x37" = New 8 bit password LSB code as desired by DIMM vendor.
5. Write to register Table 150, "Register 0x38" = New 8 bit password MSB code as desired by DIMM vendor.
6. Write to register Table 151, "Register 0x39" = 0x80.
7. Wait 200 ms.
8. Write to register Table 151, "Register 0x39" = 0x00.
9. Power cycle the PMIC. (Remove VIN_Bulk and VIN_Mgmt supply from the PMIC. The new password is in effect after the power cycle.

To change the password again from this point on, repeat steps 1 to 8 but note that in steps 1 and 2 current password is required.

Table 99 — Register 0x04

	R04		
Bits	**Attribute**	**Default**	**Description[1,2]**
7	ROE	0	R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation[3] 0 = No Error or Only 1 Error since last Erase operation 1 = > 1 Error Count since last Erase operation
6	ROE	0	R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Over or Under Voltage[4] 0 = No Error Occurred 1 = Error Occurred
5	ROE	0	R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOLTAGE Global Error Log History for VIN_Bulk Over Voltage[4] 0 = No Error Occurred 1 = Error Occurred
4	ROE	0	R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature[4] 0 = No Error Occurred 1 = Error Occurred
3:0	RV	0	R04 [3:0]: Reserved

1. The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 5.0V for VIN_Bulk voltage and 100 ms duration from PWR_GOOD signal assertion to guarantee the write operation into non-volatile memory.
2. Host must explicitly perform Erase operation to erase this entire register Table 99, “Register 0x04” [7:0] via Table 151, “Register 0x39”. The PMIC needs minimum of 100 ms for Erase operation.
3. PMIC counts the error since last erase operation and if more than one error occurs, it sets this bit to ‘1’. Host must explicitly perform Erase operation to erase this entire register Table 99, “Register 0x04” [7:0].
4. PMIC sets the bit when error occurs.